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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/798,597 | 03/10/2004 | Xiaobao Wang | 015114-054911US | 6353 |

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| EXAMINER | |
|---|---|
| CHANG, DANIEL D | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2819 | |

DATE MAILED: 10/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/798,597 | WANG ET AL. | |
| | Examiner | Art Unit | |
| | Daniel D. Chang | 2819 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *24 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *8-15,19,21 and 23-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-15,19,21,23 and 24* is/are allowed.

6)☒ Claim(s) *25-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/04/05* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

### *Acknowledgement*

Receipt is acknowledged of the Amendment filed July 24, 2006.

### *Drawings*

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the structure of multiplexers shifting two bits as claimed in claims 12 and 21 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 25-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Asano et al. (US 4719369, hereinafter "Asano").

Regarding claim 25, Asano discloses, in Figs. 1 and 2, an integrated circuit comprising:

a first pin (node between 20 and 22) coupled to connect to a resistor (22) that is external (col. 4, lines 6+) to the integrated circuit;

a first current source (20) biased by a bias voltage (gate voltage of 20) and coupled to the first pin;

an analog-to-digital converter (A/D 30 in gate width control 24) coupled to the first pin; and

a plurality of transistors (2-5 and 7-10) forming a termination impedance (col. 2, lines 58+), each coupled to one of a plurality of outputs (see 26) of the analog-to-digital converter.

Regarding claim 26, Asano discloses, in Figs. 1 and 2, that wherein the bias voltage compensates for changes in processing, supply voltage, and temperature (col. 3, lines 63+; col. 4, lines 24+, lines 47+) .

Regarding claim 27, Asano discloses, in Figs. 1 and 2, a logic circuit (31 in 24 shown in Fig. 2 and 12-15) coupled between the analog-to-digital converter and the plurality of transistors.

Regarding claim 28, Asano discloses, in Figs. 1 and 2, that wherein the logic circuit converts outputs of the analog-to-digital converter to binarily-weighted output signals (col. 4, lines 8-47).

Regarding claim 29, Asano discloses, in Figs. 1 and 2, that wherein the logic circuit output signals are binarily weighted (col. 4, lines 8-47).

Regarding claim 30, Asano discloses, in Figs. 1 and 2, that wherein the logic circuit can right shift the output signals before providing them to the output transistors, can left shift the output signals before providing them to the output transistors, or not shift the output signals before providing them to the plurality of transistors (depending on the value of the input A of the subtractor circuit 31 is set, the subtractor can right shift, left shift or not shift. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987)).

Claims 31, 32, and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Vishwanthaiah et al. (US 5,955,894, hereinafter "Vishwanthaiah").

Regarding claim 31, Vishwanthaiah discloses in Figs. 1-5, an integrated circuit comprising:

a first on-chip termination impedance circuit (212 in first driver circuit 110 in 102 as shown in Fig. 1; see Fig. 2 for detail) comprising a first plurality of parallel transistors (212, similar to pull up transistors col. 8, lines 47) coupled to a first pad (OUT coupled to the first driver circuit 110 in 102);

a first control circuit (302 in Fig. 3) coupled to adjust the termination impedance of the first on-chip termination impedance circuit by providing a first plurality of control signals (CNT BIT1U - BIT8U) to the first on-chip impedance circuit, wherein the first plurality of control signals can be right shifted, left shifted, or not shifted (depending on LEFT/RIGHT, SYSTEM CLOCK; see 506 for detail) before being provided to the first on-chip termination impedance circuit;

a second on-chip termination impedance circuit (222 in second driver circuit 110 in 102 as shown in Fig. 1; see Fig. 2 for detail) comprising a second plurality of parallel transistors coupled to a second pad (OUT coupled to the second driver circuit 110 in 102); and

a second control circuit (304 in Fig. 3) coupled to adjust the termination impedance of the second on-chip termination impedance circuit by providing a second plurality of control signals (CNT BIT1D - BIT8D) to the second on-chip impedance circuit, wherein the second plurality of control signals can be right shifted, left shifted, or not shifted (depending on LEFT/RIGHT, SYSTEM CLOCK; see 406 for detail) before being provided to the second on-chip termination impedance circuit.

Regarding claim 32, Vishwanthaiah discloses in Figs. 1-5, that wherein the first on-chip termination impedance circuit comprises a plurality of transistors (212; similar to pull up transistors col. 8, lines 47), each having a drain coupled to the first pad (OUT), and the second on-chip termination impedance comprises a plurality of transistors (222; similar to pull down transistors 422, col. 6, lines 33+), each having a drain coupled to the second pad.

Regarding claim 34, Vishwanthaiah discloses in Figs. 1-5, that wherein the first plurality of control signals are right shifted, left shifted, or not shifted, independently of whether the

second plurality of control signals are right shifted, left shifted, or not shifted (since 302 and 304 are independently operated; see 406 and 506).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vishwanthaiah in view of Haycock et al. (US 6,529,037 B1, hereinafter, "Haycock")

The teachings of Vishwanthaiah have been discussed above. Vishwanthaiah also teaches an output driver (210) connected in parallel with the first on-chip termination impedance circuit (212) but does not teach that the first on-chip termination impedance circuit coupled to a source of an output driver transistor, wherein a drain of the output driver transistor is coupled to the first pad (in another words, the output driver is connected in series with the first on-chip termination impedance circuit ).

However, Haycock teaches that wherein the first on-chip termination impedance circuit (Z, 2Z, 4Z, 8Z) is coupled to a source of an output driver transistor (320), wherein a drain of the output driver transistor is coupled to the first pad (OUT 350) in order to provide a substantially balanced output impedance.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have substituted the parallel connected output driver of Vishwanthaiah

with the series connected output driver as taught by Haycock in order to provide a substantially balanced output impedance.

### *Response to Arguments*

Applicant's arguments with respect to claims 25-34 have been considered but are moot in view of the new ground(s) of rejection.

### *Allowable Subject Matter*

Claims 8-15, 19, 21, and 23-24 are allowed.

### *Conclusion*

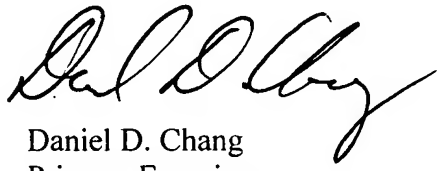
Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



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